Oxide Passivated Nanocrystalline Silicon Trap-Controlled Memory Devices

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Abstract - **An alternative to the single floating gate on a standard EEPROM device could be a continuous semi-insulating layer in which the distribution of charge can be controlled. By partial oxidation of porous silicon, a new material named Oxide Passivated Nanocrystalline Silicon (OPNSi) is formed, which has embedded Si nanocrystals in a porous glass structure. With oxide barriers between silicon nanocrystals, carriers can be confined to the silicon crystallites or trapped at interface states on the surface of these nanocrystals. With the assistance of an electric field, carriers can undergo direct tunneling through the very thin barriers and alter the charge distribution within the OPNSi layer. The placement of charge within the layer will determine the field-effect on the underlying silicon substrate. A nondestructive read would take place at low control-gate bias, and possibly result in faster write/erase cycles compared to traditional EEPROM. Another fundamental limitation of today's flash EEPROM is that each memory cell requires a pass-gate and a 3-terminal transistor structure, which limits the size of each cell. The OPNSi Diode will also be investigated as a possible candidate for a 2-terminal X-point array memory device.**

I. Objective

The purpose of this project was to investigate the feasibility of two different kinds of memory devices which use OPNSi as the "memory material". One of the memory devices studied was a traditional EEPROM-like structure, which focused on the effect of altering the charge distribution within the 0.4μm thick OPNSi film. The second approach involved investigating a two terminal cross-point array concept by investigating the effect of charge transport through the film.

II. Introduction

Traditional EEPROM memory devices involve Fowler-Nordheim (F-N) tunneling through a thin oxide layer (100 A). A control gate, which is placed above the floating gate separated by an oxide layer, controls the source to drain current and the electric field across the tunnel oxide (Figure 1). A high voltage on the control gate, such as 15V is used to increase the electric field close to 10MV/cm, which creates a steep bend in the SiO_2 energy band, forming a triangular potential barrier. Electrons then tunnel through this thinned potential barrier, upwards to the polysilicon floating-gate. Electrons are transferred back and forth between the floating gate and the substrate in order to store information. This information is read by applying a much lower voltage bias on the gate and measuring the resulting transistor current.

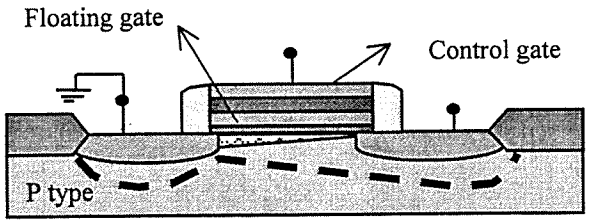

Figure 1. EEPROM – F-N tunneling

The idea behind replacing the floating gate and the thin oxide layer with OPNSi would involve the shifting of charges between silicon nanocrystals. The formation of porous silicon material introduces lots of surface area and trap sites due to the electrochemical anodization of silicon. The passivation of porous silicon with SiO2 results in a high density of interconnected silicon crystallites, separated by very thin oxide layers (Figure 2). With the assistance of an appropriate electric field, electrons tunnel through this very thin oxide (~10-15Å) layer and can transfer between the silicon crystallites. Shifting the charge distribution within this film will influence the field effect on the underlying substrate, thus controlling the threshold voltage (C-V shift) in the transistor (capacitor) structure.

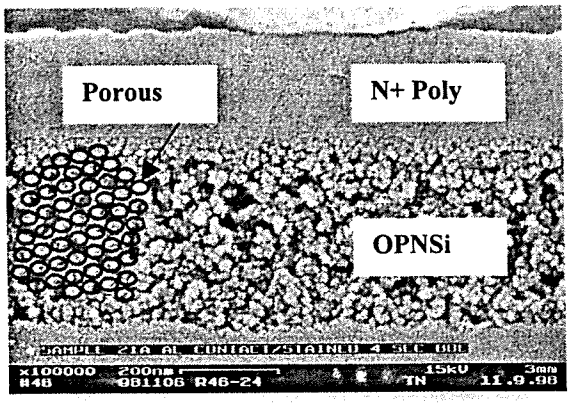

Figure 2. OPNSi Diode Structure

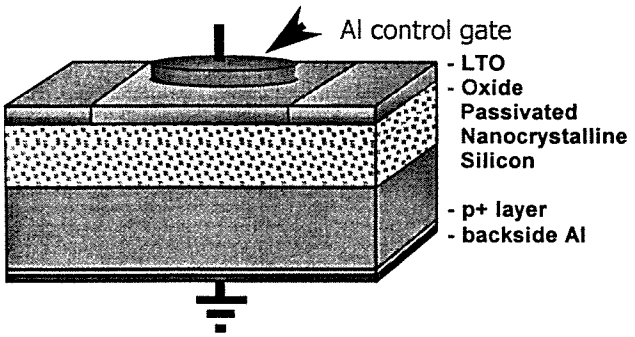

Figure 3. Fabricated Capacitor

An OPNSi capacitor was fabricated, as shown in figure 3. A high voltage is used to write/erase the device, whereas a low bias (or zero bias) can be used for a read operation. A high positive voltage (write-bias) will shift electrons up towards the OPNSi/LTO interface, causing the capacitor to remain in inversion once returned to a zero-bias condition. A high negative voltage (erase-bias) will shift the distribution of electrons toward the OPNSi/silicon interface, causing the capacitor to remain in accumulation once returned to a zero-bias condition.

Since the direct tunneling takes place at a much lower electric field as opposed to F-N tunneling, this type of structure may result in lower operating voltages and faster write/erase cycles. An OPNSi gate EEPROM may also eliminate "over-erase" problems because of self-limiting charge redistribution due to Coulombic forces.

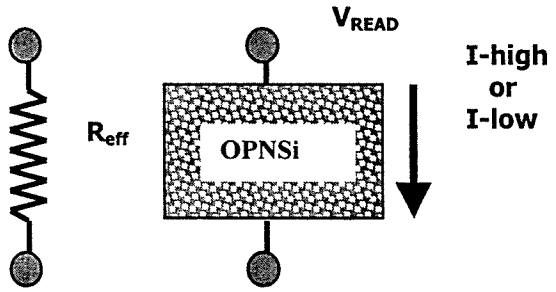

Figure 4. The Cross Point Array Concept

The cross point array concept is the idea of making a 2 terminal (gate & substrate) memory device as opposed to a 4 terminal (drain, gate, source & substrate) memory device. This concept would require an I-V hysteresis as opposed a C-V hysteresis. A reversible change in resistance may result from an adjustable level of trapped charge, resulting in different levels of charge screening, thus effecting transport in conductive pathways (Figure 4). The cross point array memory device could be programmed and read through the same two terminals, thus providing an increase in the packing density of memory cells. A change in resistance for OPNSi diodes (structure shown in figure 2) was initially observed after applying a high forward or reverse bias (see figure 5).

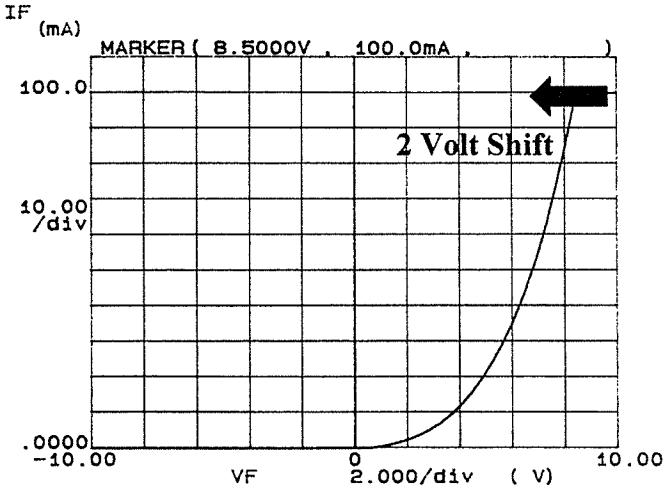

Figure 5. OPNSi Diode I-V Curve

III. Experimental Procedure

A series of experiments was designed to investigate the effects of surface disorder prior to anodization, film porosity, film thickness, passivation and the anodized substrate type on the current transport in the diode structure. Figure 5 illustrates a sample I-V curve for one of these samples. The voltage at 100mA and the differential conductance were recorded. After the analysis of the resulting data, the following conditions were determined to be the optimized values for the responses:

- Substrate Preparation
  - Induced surface disorder prior to anodization
  - 1E14 ions/cm^2 BF_2 implant
  - 900°C, 7 hours of steam oxidation
- Anodization Conditions
  - Time: 2 min.
  - Current: 135mA. (J = 3.5mA/cm^2)
- Porous silicon anneal (to form OPNSi)
  - 900°C for 15min.

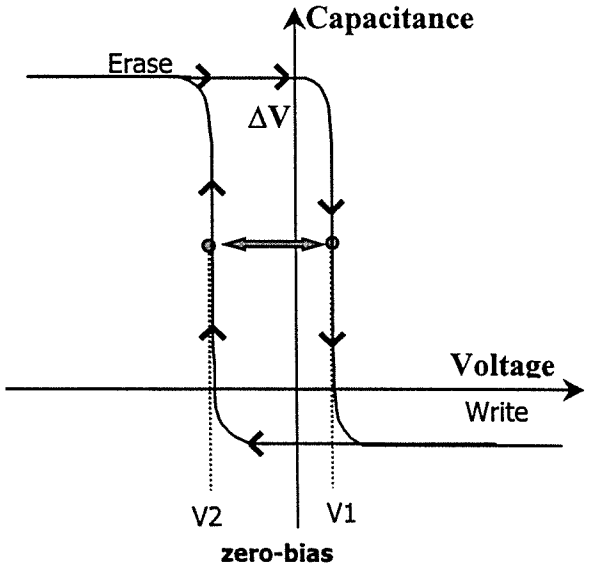

Figure 6. C-V Analysis of the Capacitor Structure

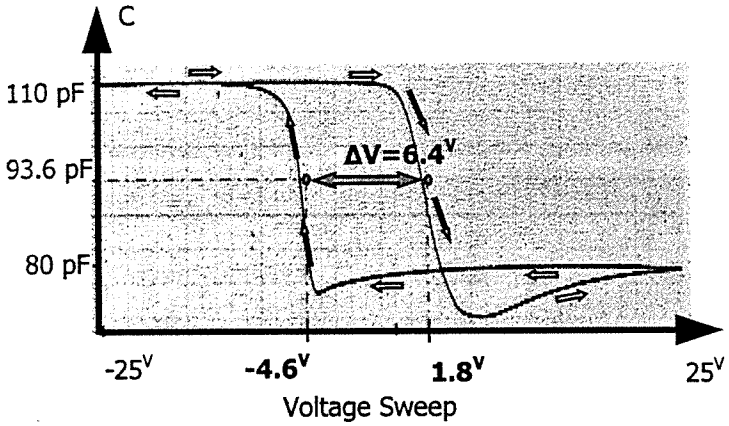

Figure 7. C-V Hysteresis

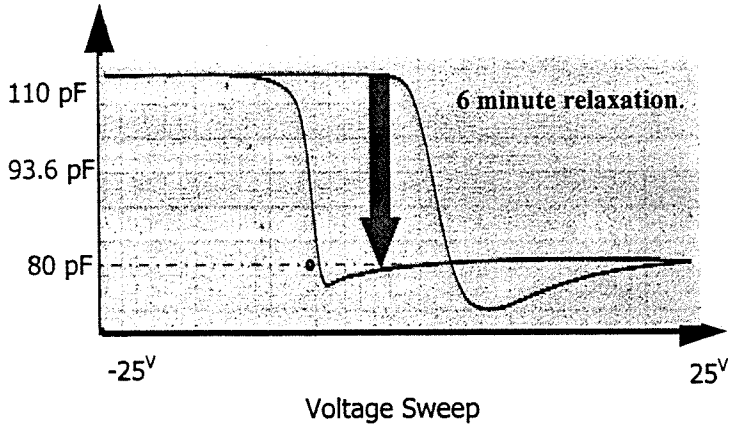

Figure 8. Charge Relaxation / Memory Loss

These optimized values were used to fabricate the desired C-V structure (Figure 5). 1200Å of low temperature oxide (LTO) film was deposited by a low-pressure chemical vapor deposition tool. This would form the insulating layer between the aluminum control gate and the OPNSi film. C-V measurements were performed on this device. A voltage sweep from –25 V to +25V was chosen to observe the C-V hysteresis. The high positive bias (+25V) was used to "write" this sample. After a minute of "write" condition, voltage was swept negative, which was also used to "erase" the device (see figure 6). After completion of this testing, zero bias testing followed in order to observe the charge relaxation tendency of our device.

IV. Results

The C-V analysis was utilized to test the functionality of this device. Initial results were very encouraging. A significant voltage shift was observed during this analysis. However , the voltage shift (ΔV) was not stable. A ΔV range of 8.6V to 2.3V (within wafer) was observed. Also, there was a variation in the measured capacitance values (130-110 pF during "write" cycle, 74-85 pF during "erase" cycle). Sample C-V curves can be seen in figure 7. Another very important observation was at "zero bias" testing. After "writing" the device was programmed to inversion (capacitance ~ 80pF), followed by erasing which programmed the device to accumulation (capacitance ~ 110pF), immediately followed by a zero-bias stability test. and pulling up the capacitance to 110pF, zero volt "read" was performed. The purpose of this "read" was to quantify the charge holding capacity of this device. After about 6 minutes of "zero bias", the capacitance relaxed back down to about 80 pF (Figure 8). This was a key issue for this device. It was possible to store information, however, the information was lost due to the relaxation/redistribution of charge within the OPNSi film.

These results were consistent with observed behavior during the I-V analysis fabricated OPNSi diodes (without the LTO). A voltage shift of around 2V at 100mA forced current was induced by a +/- 20V bias prior to the measurement. A voltage between 7.5V and 9.5V could be observed at the same current level, depending upon the preceeding bias. Although measureable, this effect was very short-lived.

V. Conclusion

The charge distribution in the OPNSi film was determined to be unstable which caused the variation in the voltage shift and capacitance values. OPNSi was also determined to be a leaky material. It took 6 minutes to discharge the capacitor and bring it to an equilibrium state (Figure 8). Also the write/erase voltages were too high (+/-25V). Writing and erasing was too long (1 min.) OPNSi does not seem feasible as a non-volatile memory device because of the unstable charge distribution nature, however, a dynamic two-terminal memory device may be feasible in the future. Fabricating more capacitor samples with an organized design of experiment will help explore the secrets of this material. Also investigating the effects of the porous silicon size on the C-V curves may be a strong lead in manufacturing these devices.

VI. Acknowledgements

I would like to thank Prof. Karl Hirschman and the department of Microelectronic Engineering at Rochester Institute of Technology for their continuous support.

VII. References

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Burcay Gurcan is from Ankara – TURKEY. He cooped for ATMEL Corporation- Colorado Springs, Advanced Vision Technologies- Rochester, and National Semiconductor- South Portland. He is a proud member of the RIT Men's Waterpolo team for 5 years, which won the New York State Championship in 1996. Burcay, will be working for National Semiconductor, South Portland, Maine after graduation.